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| EXAMINER | |
|---|---|
| COLE, BRANDON S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

| NOTIFICATION DATE | DELIVERY MODE |
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| 08/17/2009 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/589,109 | STORMS ET AL. | |
| | Examiner | Art Unit | |
| | BRANDON S. COLE | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *June 25th 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *May 14th 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/10/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/25/2009 has been entered.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 6, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al (US 2005/0017783).

As to claim 1, Lee et al figure 6 shows a voltage driver circuit for driving a device at a selected one of a plurality of voltages associated with respective device operations including a high voltage operation (E) and a relatively lower voltage operation (I), the driver circuit comprising an input (IN), a single output (OUT) for connection to said device, and a plurality of voltage drivers (610, 622, 626) between said input and said output including a high voltage breakdown driver (610, 626) and a relatively lower

breakdown voltage driver (622), wherein said high voltage breakdown driver comprises inverters and said relatively lower breakdown voltage driver comprises an inverter, wherein an output of one of the inverters of said high voltage breakdown driver is connected to an input of the inverter of said relatively lower breakdown voltage driver, the circuit being arranged such that, during a high voltage operation, said high voltage breakdown driver is connected to said output and there is a substantially zero voltage drop across said relatively lower breakdown voltage driver, and, during a relatively lower voltage operation, said relatively lower breakdown voltage driver provides the drive voltage for driving said device, the contribution of said high breakdown voltage driver to said drive voltage during said relatively lower voltage operation being substantially negligible. Note that, for the functional limitation "during a high voltage operation, said high voltage breakdown driver-is connected to said output and there is a substantially zero voltage drop across said relatively lower breakdown voltage driver" recited in claim 1, because the structure of the claim is fully shown in figure, then the operation of the circuitry in Lee et al figure 6 also meets all the functional limitations (see MPEP 2114, and In re Schreiber, 128 F.3d 1473, 44 USPQ2d 1429 (Fed. Cir. 1997)).

As to claim 4, Lee et al figure 6 shows a voltage driver circuit comprising two signal paths between the input (IN) and the output (OUT), a first signal path (NK) consisting of one or more high voltage drivers (626) connected in series, and a second signal path (NJ) consisting of at least one low voltage drive (622), the first and second signal paths being connected in parallel to one another.

Claim 6 has similar limitations as claim 1. Therefore, the claim is rejected for the same reasons.

As to claim 11,Lee et al figure 8 shows a high voltage pull-up transistor (625) that is provided between the first voltage line (EVC) and the output (OUT).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 2005/0017783) in view of Huang (US 2005/0156631).

As to claim 2, Lee et al figure 6 shows a circuit wherein said high voltage breakdown driver consists of inverters (610, 626).

Lee et al fails to show that the inverters of said high voltage breakdown driver consisting of high voltage breakdown transistors.

However, Huang figure 2 shows inverters of said high voltage breakdown driver (23) consists of high voltage breakdown transistors. Huang teaches in paragraph [0020] that inverters of circuit 23 comprise high-voltage devices.

Therefore, it would have been obvious for one having ordinary skill in the art, at the time of the invention to replace Lee et al's high voltage breakdown driver consisting of inverters with Huang's high voltage breakdown driver consisting of inverters comprising of high voltage breakdown transistors for the purpose of providing a balanced duty cycle and increase circuit reliability and operations stability.

As to claim 3, Lee et al figure 6 shows a circuit wherein said low voltage breakdown driver consist of an inverter (622).

Lee et al fails to show that the inverters of said low voltage breakdown driver consists of low voltage breakdown transistors.

However, Huang figure 2 shows inverter of said low voltage breakdown driver (21) consists of low voltage breakdown transistors. Huang teaches in paragraph [0018] that inverter in circuit 21 operate at a low voltage.

Therefore, it would have been obvious for one having ordinary skill in the art, at the time of the invention to replace Lee et al's low voltage breakdown driver consisting

an inverter with Huang's low voltage breakdown driver consisting an inverter comprising of low voltage breakdown transistors for the same reasons as above.

7. Claims 5, 7, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 2005/0017783) in view of Mentze et al (US 7,030,654).

As to claim 5, Lee et al figure 6 shows a voltage driver circuit comprising two signal paths (NK, NJ) between the input (IN) and the output (OUT).

Lee et al fails to show that the circuit comprises a means for selecting the first signal path during high voltage operation.

However, Mentze et al figure 1 shows a circuit according to claim 1 comprising a means for selecting the first signal path during high voltage operation. Mentze et al teaches column 3, lines 24 – 27 that input signal resides between two logic levels (Wikipedia - Clock Signal) so that when the logic level is high the first signal path is selected.

Therefore, it would have been obvious for one having ordinary skill in the art to use Mentze et al's means for selecting a first path for Lee et al's first and second path for the purpose of controlling high voltage signals that exceed breakdown voltage of the process.

As to claim 7, Lee et al figure 6 shows a voltage level shifter (610, 626) but fails to show that the voltage level shifter comprises of a partial level shifter.

However, Mentze et al figure 2 shows that the voltage level shifter comprises of a partial level shifter (208, 210, 212, and 214). The level shifter is partial because it only connects to VddH and VddL, it cannot support the full voltage drop of VDDH to Ground. Mentze et al teaches in column 4, lines 53 – 54 that the high voltage buffer stage is tied between VddL and Vddh.

Therefore, it would have been obvious for one having ordinary skill in the art to use r Lee et al's voltage level shifter with Mentze et al's partial level shifter for the same reasons as above.

As to claim 15, Mentze et al figure 2 shows a circuit wherein source electrodes of some high voltage breakdown transistors (218) and a source electrode of a first relatively lower breakdown voltage transistor (20) are connected to a first voltage line (VddL), wherein source electrodes of some other high voltage breakdown transistors (212, 214) and a source electrode of a second relatively lower breakdown voltage transistor are connected to a second voltage line (Ground). It would have been obvious for high voltage breakdown transistors and a source electrode of a first relatively lower breakdown voltage transistor are connected to a first voltage line, wherein source electrodes of some other high voltage breakdown transistors and a source electrode of a second relatively lower breakdown voltage transistor are connected to a second voltage line, for the same reasons as above.

8. Claims 8 -10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 2005/0017783) in view of Chen et al (US 7,193,441).

As to claims 8 and 9, Lee et al figure 6 further shows a relatively lower breakdown voltage driver (622) comprising of an inverter

Lee et al fails to show that the inverter consisting of thick gate oxide devices ($GO_2$ is the same thing as a thick gate oxide device (Taught in Schoellkopf et al (US 2006/0054952) paragraph [0060])).

However, Chen et al teaches in column 3, lines 27 – 36 that inverter connected to the input signal a utilize thick gate oxide layer to protect to prevent gate oxide breakdown.

Therefore, it would have been obvious for one having ordinary skill in the art, at the time of the invention, to use Chen et al's inverters in place of Lee et al's inverters with the purpose of preventing gate oxide breakdown.

Claim 10 has similar limitations as to claim 8 above (the thick oxide layer protects the input inverter). Therefore, the claim is rejectted for the same reasons.

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 2005/0017783) in view of Chen et al (US 7,193,441), as applied to claim 8, in further view of Mentze et al (US 7,030,654).

Lee et al figure 2 shows a high voltage breakdown voltage driver (610, 626) and a low voltage breakdown voltage driver (622).

However, Lee et al and Chen et al fails to a show high voltage breakdown transistors and a source electrode of a first relatively lower breakdown voltage transistor are connected to a first voltage line, wherein source electrodes of some other high voltage breakdown transistors and a source electrode of a second relatively lower breakdown voltage transistor are connected to a second voltage line, for the same reasons as above.

However, Mentze et al figure 2 shows a circuit wherein source electrodes of some high voltage breakdown transistors (218) and a source electrode of a first relatively lower breakdown voltage transistor (20) are connected to a first voltage line (VddL), wherein source electrodes of some other high voltage breakdown transistors (212, 214) and a source electrode of a second relatively lower breakdown voltage transistor are connected to a second voltage line (Ground). Mentze et al column 3, line 21 that the circuit comprises high and low voltage buffer stages.

Therefore, it would have been obvious for one having ordinary skill in the art, at the time of the invention, to replace Lee et al's high voltage breakdown voltage driver and low voltage breakdown voltage driver with Mentze et al's high voltage breakdown voltage driver and low voltage breakdown voltage driver for the purpose of providing a balanced duty cycle and increase circuit reliability and operations stability

10. Claims 12 -14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al (US 2005/0017783) as applied to claim 1 above, and in further of Rhee (US 2001/0000949).

As to claims 12 and 13 Lee et al fails to teach that the voltage driver circuit is part of memory device.

However, Rhee figure 5 teaches in paragraph [0011] that the driver circuit is used in an integrated circuit memory device.

Therefore it would have been obvious to one having ordinary skill in the art, at the time of the invention to use Lee et al's voltage driver circuit in an integrated circuit memory device for the purpose of accounting for variations in loading of the memory device.

Claim 14 has similar limitations as to claim 13 above (an integrated circuit is a type of a computing system (Wikipedia – Integrated Circuits)). Therefore, the claim is rejected for the same reasons.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. COLE whose telephone number is (571)270-5075. The examiner can normally be reached on Mon - Fri 7:30-5:00 EST (Alternate Friday's Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brandon S Cole/
Examiner, Art Unit 2816
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